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OBJECTIVE

Seeking internship for Hardware/Firmware Engineer role to apply my knowledge in low-level programming, embedded systems, RTOS, PCB layout and and system-level debugging to develop next generation embedded and discrete platforms.

EXPERIENCE

Quantum Computing Inc May 2025 – Present
Hardware Engineer Intern Hoboken, NJ

- Developed hardware for high-speed power measurement for a Quantum Entropy Computer using NXP IMXRT 1060 (ARM Cortex-M7), achieving 10 MSPS sampling to capture precise power consumption data in real time.
- Wrote low-level firmware in C/C++ to interface a parallel high-speed ADC, managing precise timers control, DMA, GPIO synchronization (FlexIO). PCB design with safety isolation and EMI filtering principles under RF-speed constrains.
- Designed and tested the front-end hardware from component selection to PCB design in Altium Designer, voltage/current sensing, and system level debugging using oscilloscope and logic analyzer, applied EMI-aware layout practices.

San Francisco State University Jan 2025 – May 2025
Graduate Research Assistant San Francisco, CA

- Automated SPICE/HSPICE simulations for measurement o distributed RC interconnects using Python, extracting delay, slew, and tail metrics across varying resistance, capacitance, and segmentation conditions and built admittance-based reduced-order Pi models, achieving <5% error vs. full RC trees, improving EDA tool efficiency for timing.
- Validated models with HSPICE and implemented a machine learning to identify cases needing higher-order delay modeling for accurate interconnect prediction. Python for data parsing, plotting and analysis of large dataset.

Tirex Chargers Jan 2024 – May 2024
Embedded Hardware Intern Ahmedabad, India

- Designed hardware boards (PCB Schematic & Layout) for AC chargers utilizing Altium, focusing regulators, Power and Load regulation Achieved 15% smaller board size by placement and routing, and synthesized circuits in LTSpice.
- Executed test plans for PCBA bring-up boards, resolving 20+ design flaws (signal integrity, power, thermal), maximized stability by 20% and system validation with ATE (Automated Test Equipment) like oscilloscopes and spectrum analyzers.
- Build low level embedded software for UHF-RFID drivers and sensor/actuator integration with UART, I2C, SPI on ARM Linux system. Also utilized MATLAB Simulink and ML to model Buck/Boost converters with PI control for <5% noise.

SKILLS

- **Programming Language:** MATLAB, C, C++, Python (test automation, data analysis, plotting), Verilog
- **Systems:** Real Time Operating System (RTOS), Linux OS Scripting, Windows, Bare-metal programming, RISC-V
- **Design Automation Tools:** Synopsys Custom Compiler (Similar to Cadence Virtuoso), VCS, IC Compiler (ICC2), LTSpice, PrimeTime, HSpice, WaveView, Design Compiler, Xilinx ISE, MATLAB, MultiSim, Altium
- **Microcontrollers:** STM32L476, STM32G4, 8086, Arduino, Teensy 4.1, ESP32/ESP8266, Raspberry PI
- **Communication Protocol:** UART, I2C, SPI, USB, CAN, RF (BLE, Wi-Fi), TCP/IP, UDP, Ethernet, OCPP, MQTT
- **Measurement Tools:** Multimeter, Logic Analyzer, Spectrum Analyzer, Oscilloscope, Waveform Generator, VNA

PROJECTS

Custom RTOS on Microcontroller STM32L476 |

- Build an bare-metal ARM Cortex-M4 RTOS from scratch, including SysTick-based task scheduling, context switching, synchronization, inter-task communication, semaphores, interrupt handling, DMA and memory optimization.
- Designed a priority-based, pre-emptive RTOS scheduler within the kernel, supporting Round Robin, Cooperative, and Periodic scheduling for task management and context switching. Integrated Peripheral drivers and debugged using SWD.

Custom Standard Cell Library Design in 14nm FinFET Technology | Custom Compiler, HSpice

- Developed individual layout for basic gates such as NAND, NOR, Inverter, XOR and verified timing properties.
- Tested timing characteristics under different temperatures with HSPICE simulations for pre- and post-layout analysis.
- Carried out DRC, LVS, and parasitic extraction on each standard cell and crafted corresponding symbols.

16 x 18 SRAM Design in 14nm = FinFET Technology | Custom Compiler, WaveView.

- Constructed SRAM wrapper that includes Precharge circuit, write driver, Sense amp, Address Decoder & SRAM cell, created schematic and layout with are of 624 μm^2(optimized for area).
- Carried top-level functional verification, calculated and minimized for access time, and active power, cleared LVS & DRC.

EDUCATION

San Francisco State University, San Francisco, CA May 2026 (Expected)
Master of Science, Electrical and Computer Engineering GPA: 3.8 / 4.0
Courses: Embedded System, ASIC Design, Neural Machine Interface, Hardware for Machine Learning

Gujarat Technological University, Ahmedabad, India May 2024
Bachelor of Engineering, Electronics and Communication GPA: 3.76 / 4.0